

FIG. 1

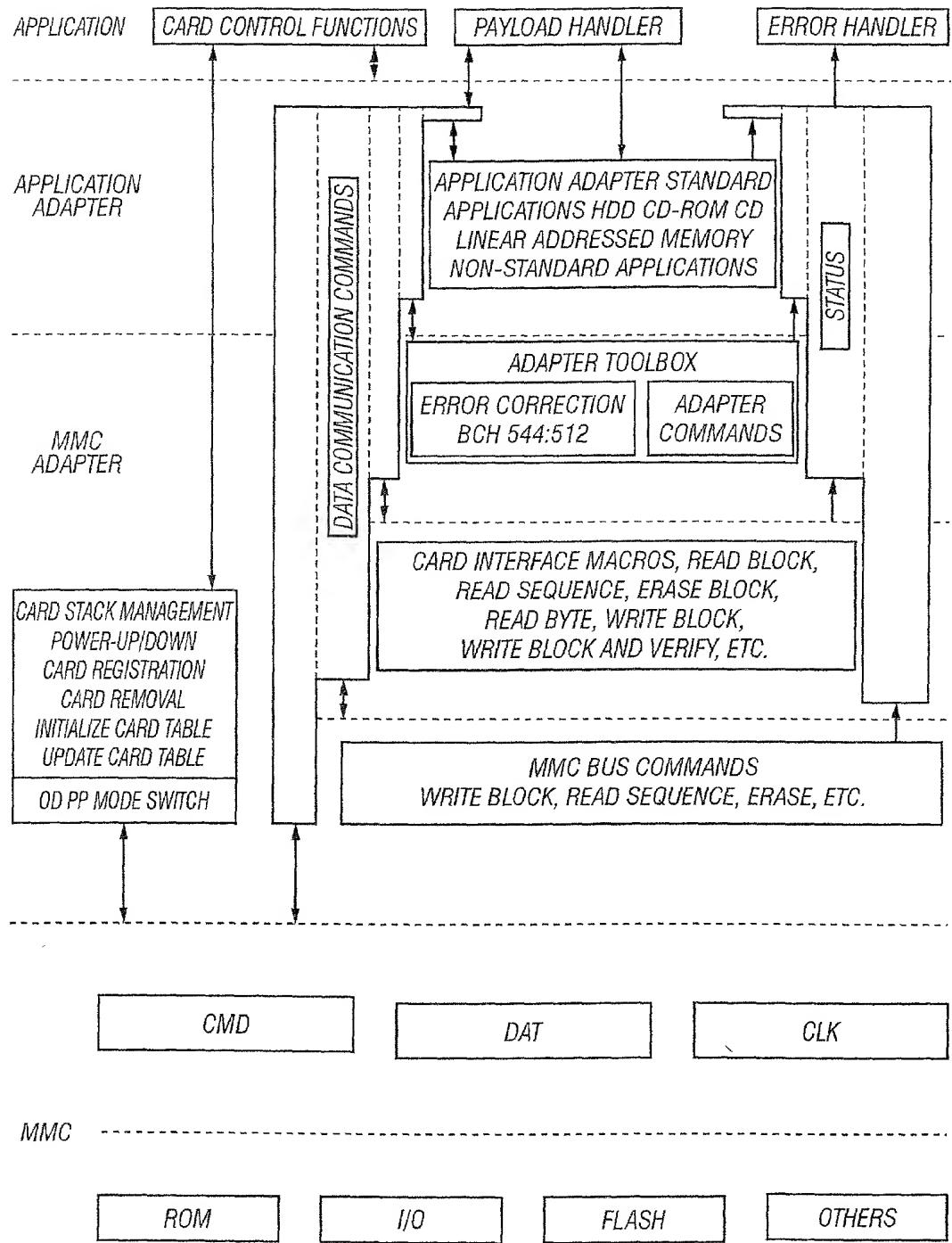


FIG. 2

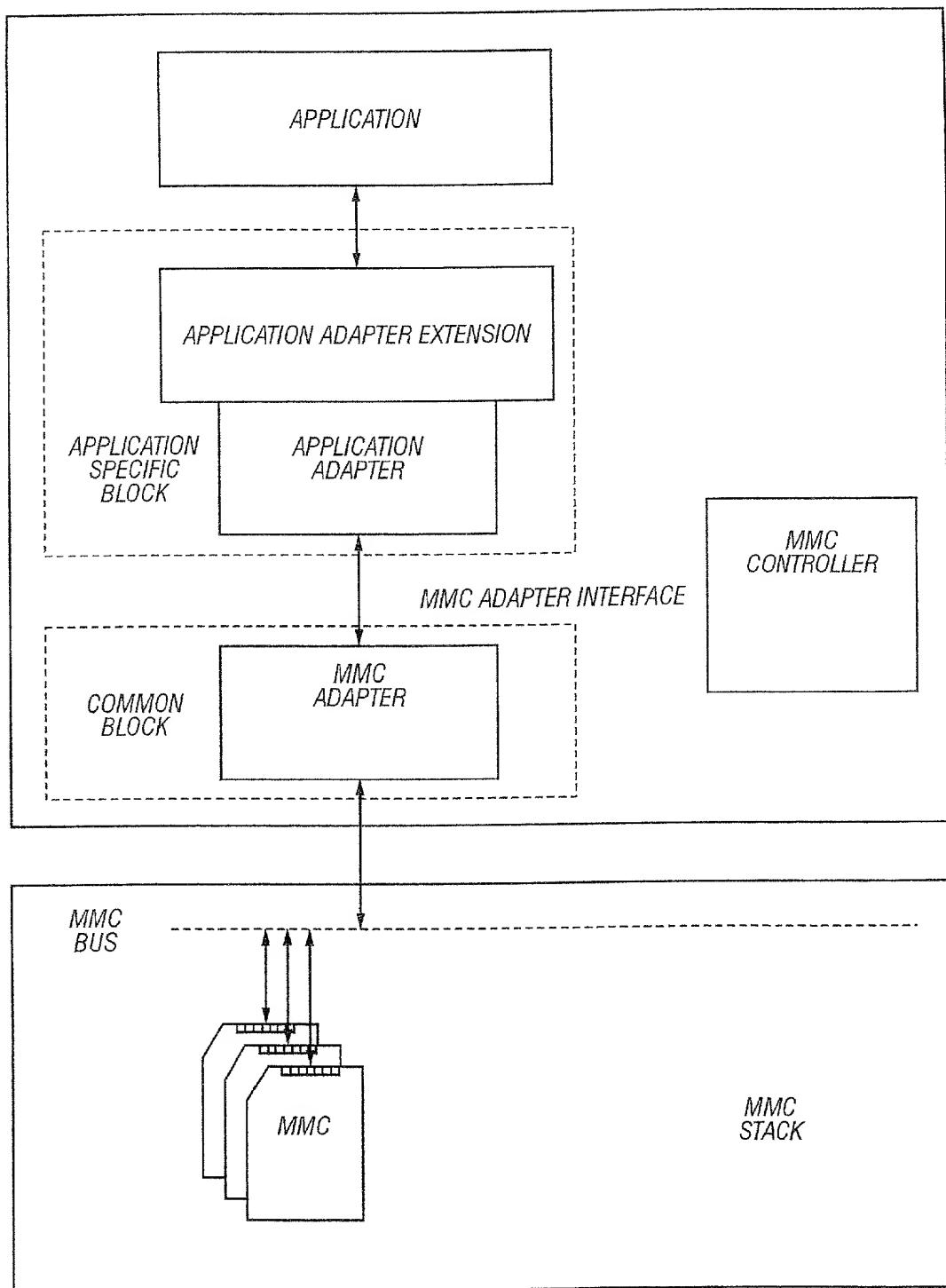


FIG. 3

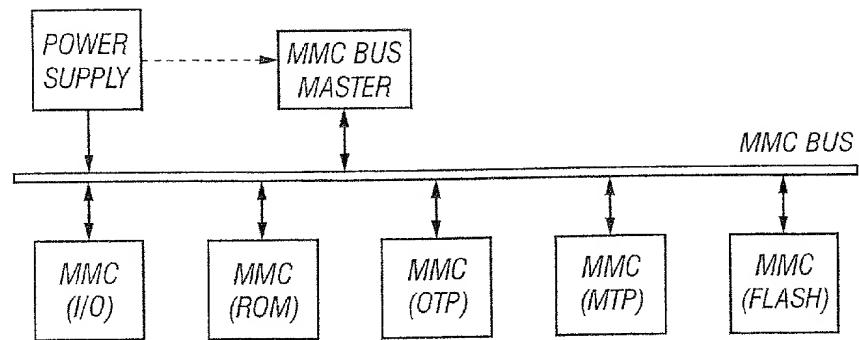


FIG. 4

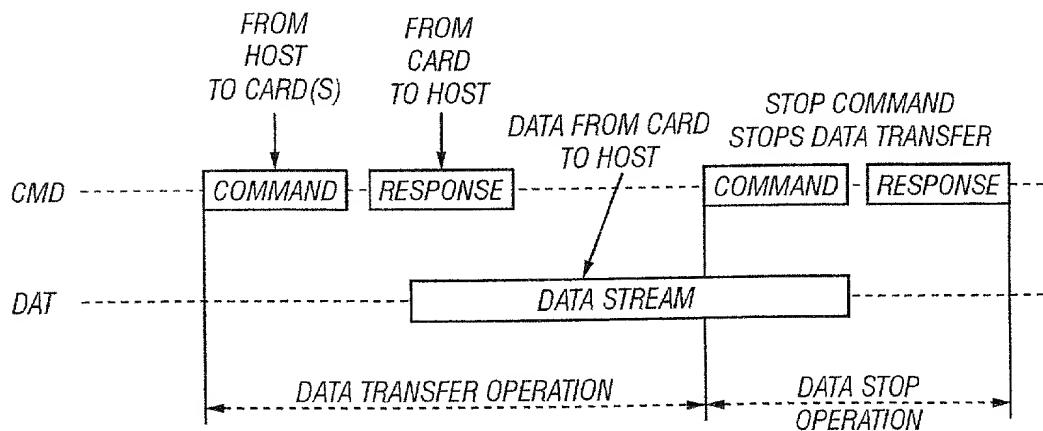


FIG. 5

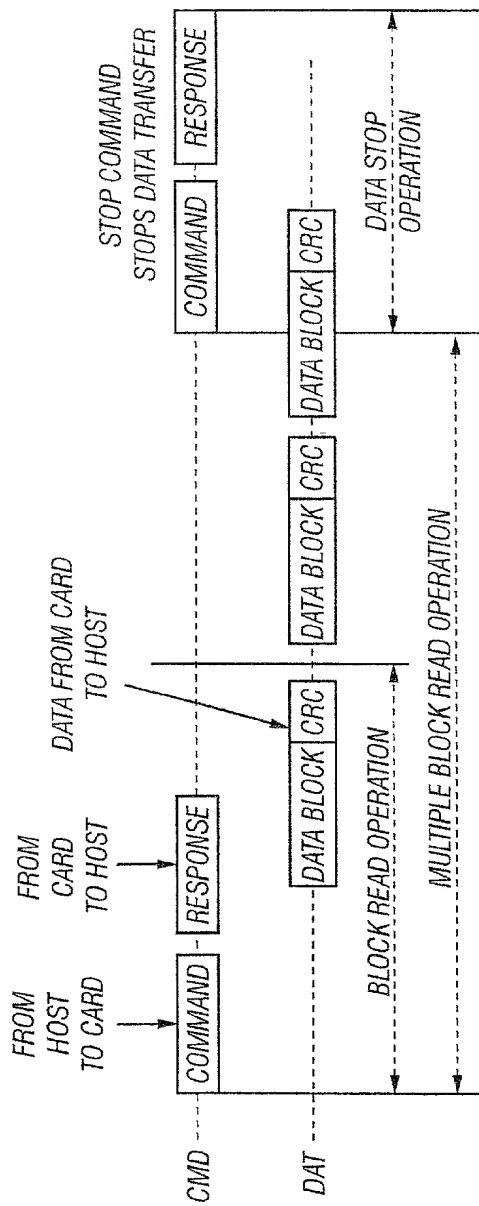


FIG. 6

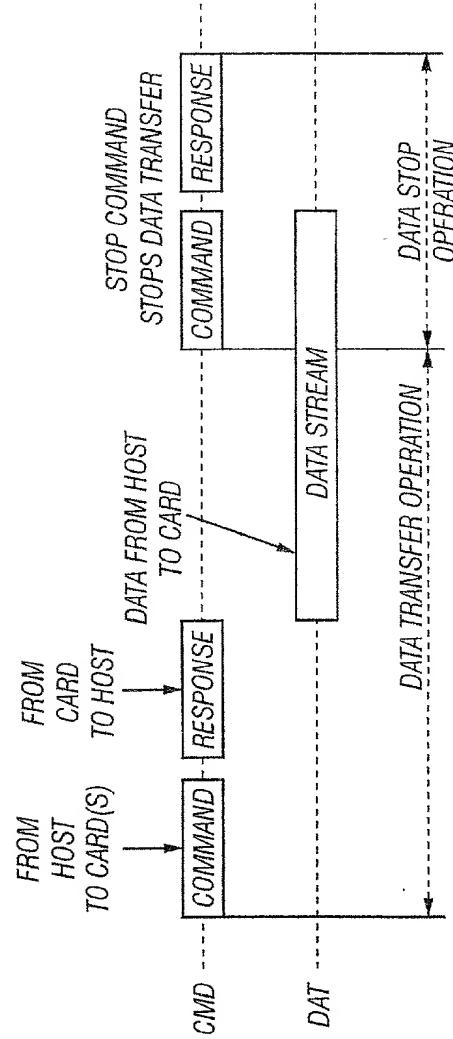


FIG. 7

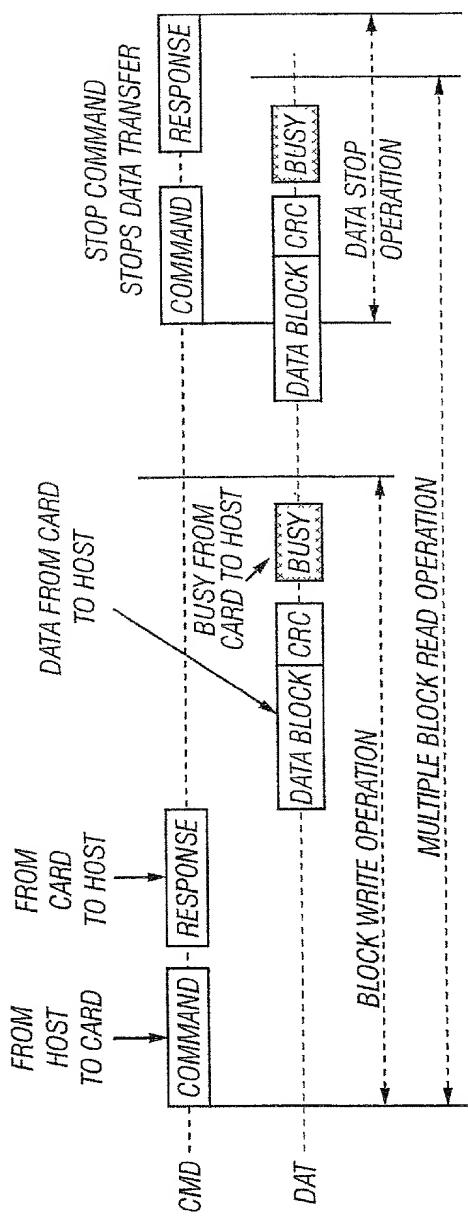


FIG. 8

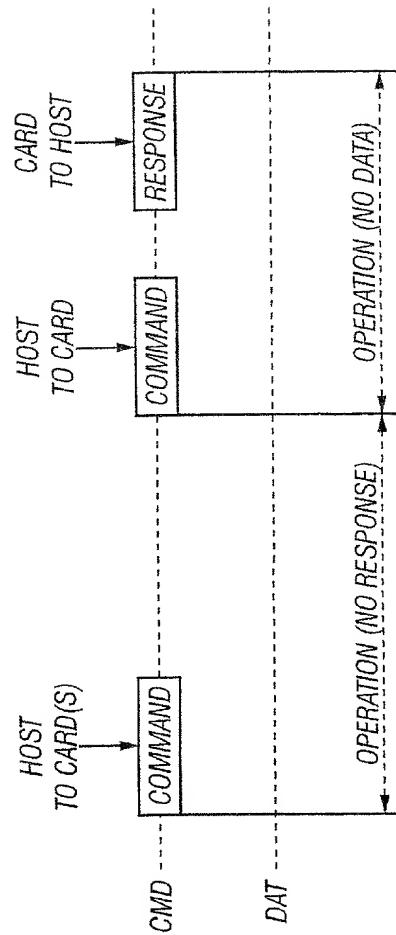


FIG. 9

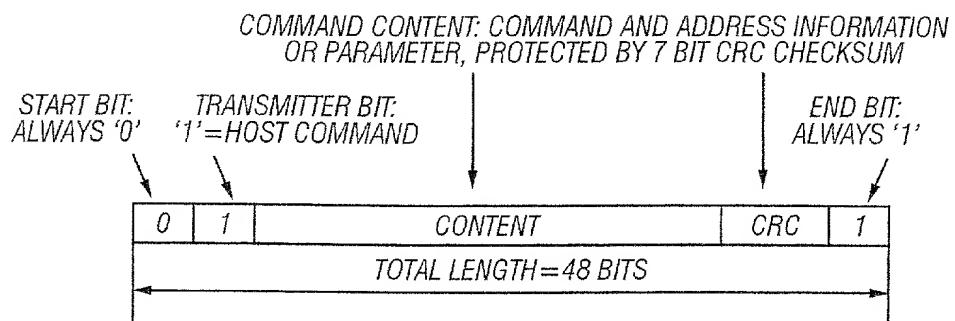


FIG. 10

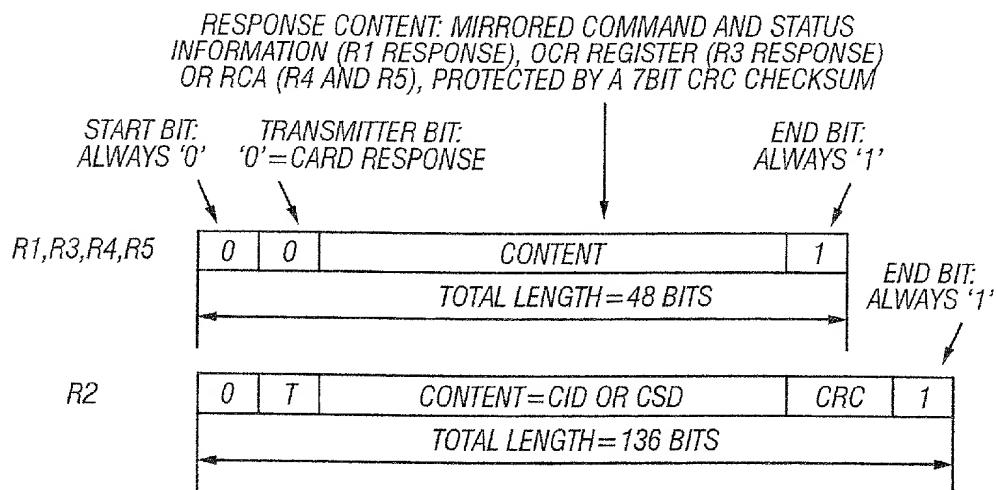


FIG. 11

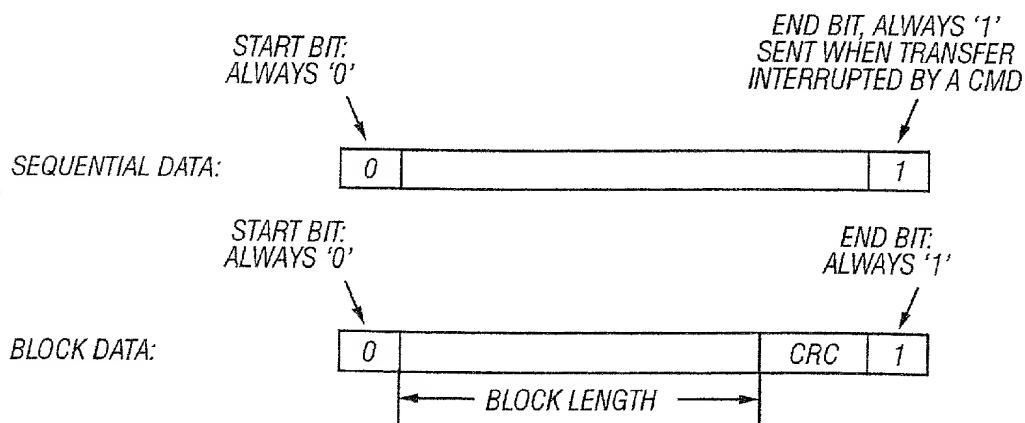


FIG. 12

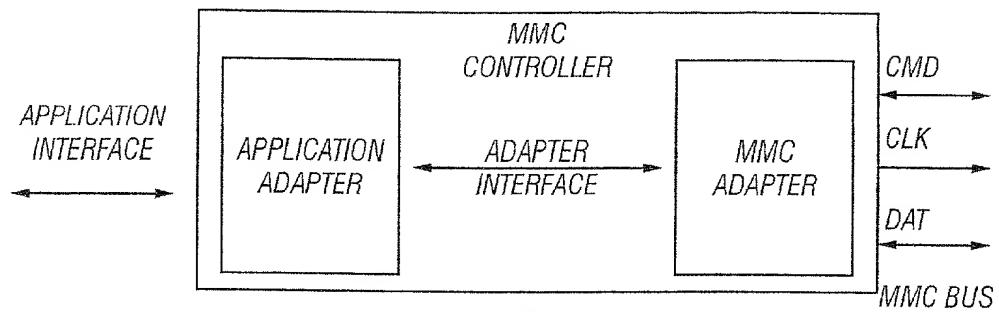


FIG. 13

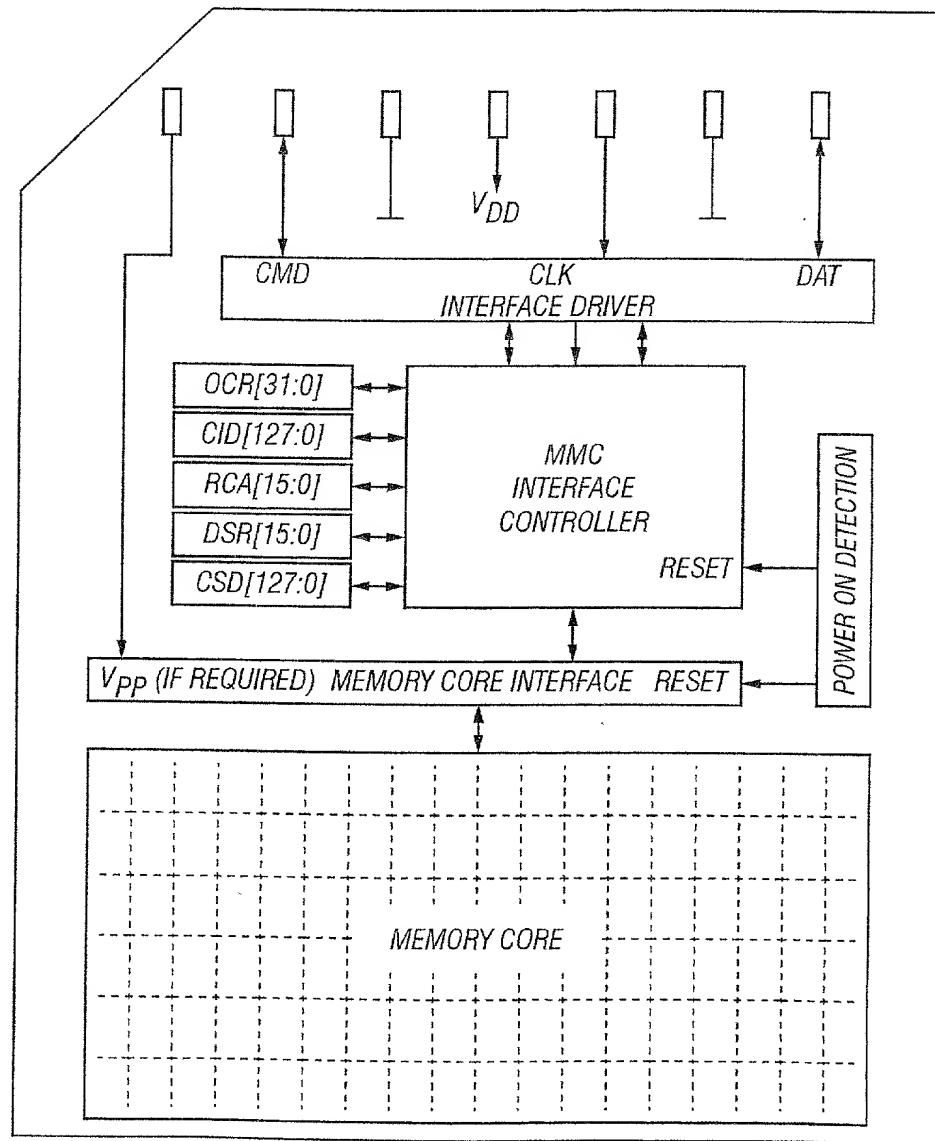


FIG. 14

OCR BIT POSITION	VDD VOLTAGE WINDOW
0-7	RESERVED
8	2.0-2.1
9	2.1-2.2
10	2.2-2.3
11	2.3-2.4
12	2.4-2.5
13	2.5-2.6
14	2.6-2.7
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-30	RESERVED
31	CARD POWER UP STATUS BIT (BUSY) ¹

1)THIS BIT IS SET TO LOW IF THE CARD HAS NOT FINISHED THE POWER UP ROUTINE

FIG. 15

NAME	FIELD	WIDTH	CID-SLICE
MANUFACTURER ID	MID	24	[127:104]
CARD INDIVIDUAL NUMBER	CIN	96	[103:8]
CRC7 CHECKSUM	CRC	7	[7:1]
NOT USED, ALWAYS '1'	-	1	[0:0]

FIG. 16

NAME	FIELD	WIDTH	CELL TYPE	CSD-SLICE
CSD STRUCTURE	CSD_STRUCTURE	2	R	[127:126]
MMC PROTOCOL VERSION	MMC_PROT	4	R	[125:122]
RESERVED	-	2	R	[121:120]
DATA READ ACCESS-TIME-1	TAAC	8	R	[119:112]
DATA READ ACCESS-TIME-2 IN CLK CYCLES (NSAC*100)	NSAC	8	R	[111:104]
MAX. DATA TRANSFER RATE	TRAN_SPEED	8	R	[103:96]
CARD COMMAND CLASSES	CCC	12	R	[95:84]
MAX. READ DATA BLOCK LENGTH	READ_BL_LEN	4	R	[83:80]
PARTIAL BLOCKS FOR READ ALLOWED	READ_BL_PARTIAL	1	R	[79:79]
WRITE BLOCK MISALIGNMENT	WRITE_BLK_MISALIGN	1	R	[78:78]
READ BLOCK MISALIGNMENT	READ_BLK_MISALIGN	1	R	[77:77]
DSR IMPLEMENTED	DSR_IMP	1	R	[76:76]
EXTERNAL V_{PP}	VPROG	2	R	[75:74]
DEVICE SIZE MANTISSA	C_SIZE_MANT	8	R	[73:66]
DEVICE SIZE EXPONENT	C_SIZE_EXP	4	R	[65:62]
MAX. READ CURRENT @ V_{DD} MIN	VDD_R_CURR_MIN	3	R	[61:59]
MAX. READ CURRENT @ V_{DD} MAX	VDD_R_CURR_MAX	3	R	[58:56]

FIG. 17A

NAME	FIELD	WIDTH	CELL TYPE	CSD-SLICE
MAX. WRITE CURRENT @ V_{DD} MIN	VDD_W_CURR_MIN	3	R	[55:53]
MAX. WRITE CURRENT @ V_{DD} MAX	VDD_W_CURR_MAX	3	R	[52:50]
MAX. V_{PP} CURRENT	VPP_CURR	3	R	[49:47]
ERASE SECTOR SIZE	SECTOR_SIZE	5	R	[46:42]
ERASE GROUP SIZE	ERASE_GRP_SIZE	5	R	[41:37]
WRITE PROTECT GROUP SIZE	WP_GRP_SIZE	5	R	[36:32]
WRITE PROTECT GROUP ENABLE	WP_GRP_ENABLE	1	R	[31:31]
MANUFACTURER DEFAULT ECC	DEFAULT_ECC	2	R	[30:29]
STREAM WRITE SPEED FACTOR	R2W_FACTOR	3	R	[28:26]
MAX. WRITE DATA BLOCK LENGTH	WRITE_BL_LEN	4	R	[25:22]
PARTIAL BLOCKS FOR WRITE ALLOWED	WRITE_BL_PARTIAL	1	R	[21:21]
RESERVED	-	5	R	[20:16]
RESERVED	-	3	R/W	[15:13]
COPY FLAG (OTP)	COPY	1	R/W	[12:12]
PERMANENT WRITE PROTECTION	PERM_WRITE_PROTECT	1	R/W	[11:11]
TEMPORARY WRITE PROTECTION	TMP_WRITE_PROTECT	1	R/W/E	[10:10]
ECC CODE	ECC	2	R/W/E	[9:8]
CRC	CRC	7	R/W/E	[7:1]
NOT USED, ALWAYS '1'	-	1	-	[0-0]

FIG. 17B

CSD_STRUCTURE	CSD STRUCTURE VERSION	VALID FOR MMC PROTOCOL VERSION
0	CSD VERSION NO. 1.0	MMC PROTOCOL VERSION 1.0-1.2
1	CSD VERSION 1.1	MMC PROTOCOL VERSION 1.4
2-3	RESERVED	

FIG. 18

MMC_PROT	MMC PROTOCOL VERSION
0	MMC PROTOCOL VERSION 1.0-1.2
1	MMC PROTOCOL VERSION 1.3
2-15	RESERVED

FIG. 19

TAAC BIT POSITION	CODE
2:0	TIME EXPONENT 0=1NS, 1=10NS, 2=100NS, 3=1μμS, 4=10μμS, 5=100μμS, 6=1MS, 7=10MS
6:3	TIME MANTISSA 0=RESERVED, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5 B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	RESERVED

FIG. 20

TRAN_SPEED BIT	CODE
2:0	TRANSFER RAE EXPONENT 0=100KBIT/S, 1=1MBIT/S, 2=10MBIT/S, 3=100MBIT/S, 4...7=RESERVED
6:3	TIME MANTISSA 0=RESERVED, 1=1.0, 2=1.2, 3=1.3, 4=1.5 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5 B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	RESERVED

FIG. 21

CCC BIT	SUPPORTED CARD COMMAND CLASS
0	CLASS 0
1	CLASS 1
.....	
11	CLASS 11

FIG. 22

BL_LEN	BLOCK LENGTH	REMARK
0	$2^0 = 1\text{ BYTE}$	
1	$2^1 = 2\text{ BYTES}$	
....		
11	$2^{11} = 2048\text{ BYTES}$	
12-14	RESERVED	
15	ANY	CAN BE SET BY THE HOST IN 1 BYTE STEPS BETWEEN 1 BYTE AND (THEORETICALLY) THE TOTAL DEVICE SIZE

FIG. 23

DSR_IMP	DSR TYPE
0	NO DSR IMPLEMENTED
1	DSR IMPLEMENTED

FIG. 24

<i>VDD_R_CURR_MIN</i> <i>VDD_W_CURR_MIN</i>	CODE FOR CURRENT CONSUMPTION @ V_{DD}
2:0	$0=0.5mA; 1=1mA; 2=5mA; 3=10mA; 4=25mA;$ $5=35mA; 6=60mA; 7=100mA$
<i>VDD_R_CURR_MAX</i> <i>VDD_W_CURR_MAX</i>	CODE FOR CURRENT CONSUMPTION @ V_{DD}
2:0	$0=1mA; 1=5mA; 2=10mA; 3=25mA; 4=35mA;$ $5=45mA; 6=80mA; 7=200mA$

FIG. 25

<i>R2W_FACTOR</i>	<i>MULTIPLES OF READ ACCESS TIME</i>
0	1
1	2 (WRITE HALF AS FAST AS READ)
2	4
3	8
4	16
5	32
6,7	<i>RESERVED</i>

FIG. 26

<i>ECC</i>	<i>ECC TYPE</i>	<i>MAXIMUM NUMBER OF CORRECTABLE BITS PER BLOCK</i>
0	<i>NONE (DEFAULT)</i>	<i>NONE</i>
1	<i>BCH (542,512)</i>	3
2-3	<i>RESERVED</i>	-

FIG. 27

CSD FIELD	COMMAND CLASSES									
	0	1	2	3	4	5	6	7	8	9
CSD_STRUCTURE	+	+	+	+	+	+	+	+	+	+
MMC_PROT	+	+	+	+	+	+	+	+	+	+
TAAC		+	+	+	+	+	+	+	+	
NSAC		+	+	+	+	+	+	+	+	
TRAN_SPEED		+	+	+	+					
CCC	+	+	+	+	+	+	+	+	+	+
READ_BL_LEN			+							
READ_BL_PARTIAL			+							
WRITE_BL_MISALIGN					+					
READ_BL_MISALIGN				+						
DSR_IMP	+	+	+	+	+	+	+	+	+	+
VPROG				+	+	+	+	+	+	
C_SIZE_MANT		+	+	+	+	+	+	+	+	
C_SIZE_EXP		+	+	+	+	+	+	+	+	
VDD_R_CURR_MIN		+	+							
VDD_R_CURR_MAX		+	+							
VDD_W_CURR_MIN				+	+	+	+	+	+	
VDD_W_CURR_MAX				+	+	+	+	+	+	
VPP_CURR				+	+	+	+	+	+	
SECTOR_SIZE					+	+	+	+		
ERASE_GRP_SIZE					+	+	+	+		
WP_GRP_SIZE						+	+	+		
WP_GRP_ENABLE						+	+	+		
DEFAULT_ECC	+	+	+	+	+	+	+	+	+	
R2W_FACTOR				+	+	+	+	+	+	
WRITE_BL_LEN				+	+	+	+	+	+	
WRITE_BL_PARTIAL				+	+	+	+	+	+	
COPY	+	+	+	+	+	+	+	+	+	+
PERM_WRITE_PROTECT	+	+	+	+	+	+	+	+	+	+
TMP_WRITE_PROTECT	+	+	+	+	+	+	+	+	+	+
ECC		+	+	+	+	+	+	+	+	
CRC	+	+	+	+	+	+	+	+	+	+

FIG. 28

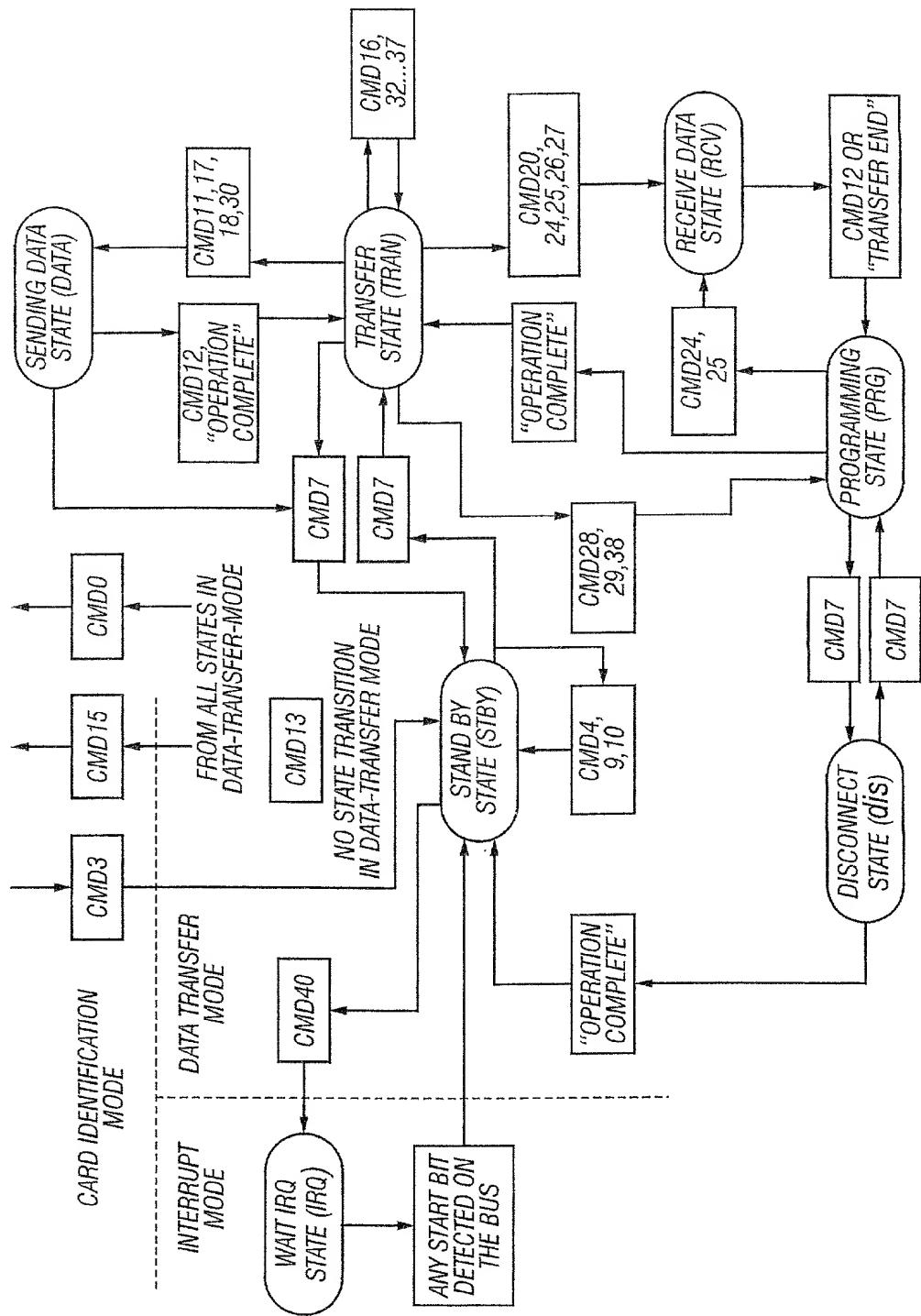


FIG. 29

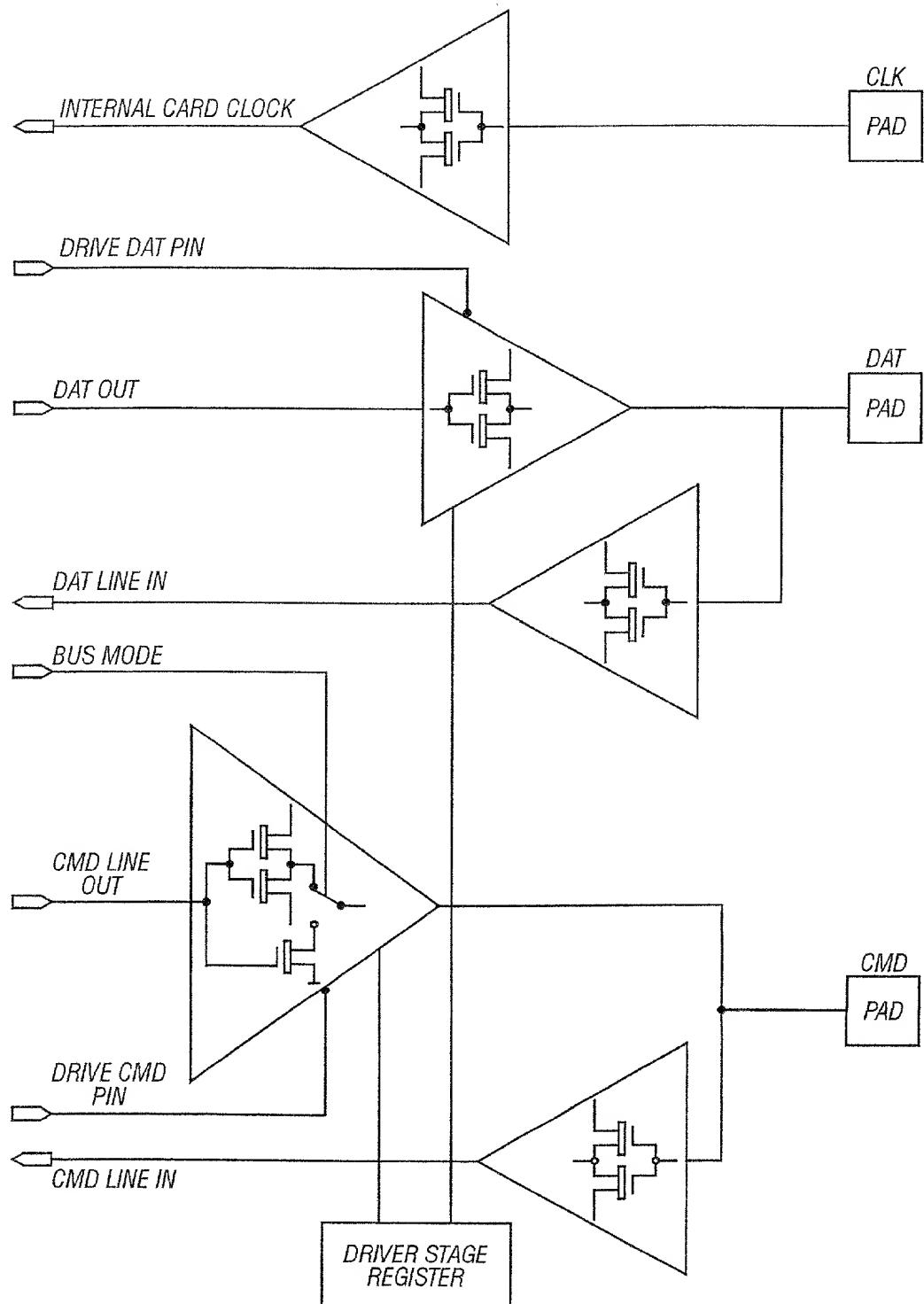


FIG. 30

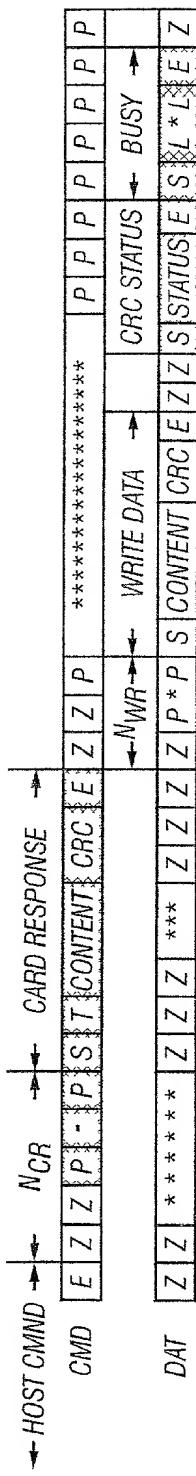


FIG. 31

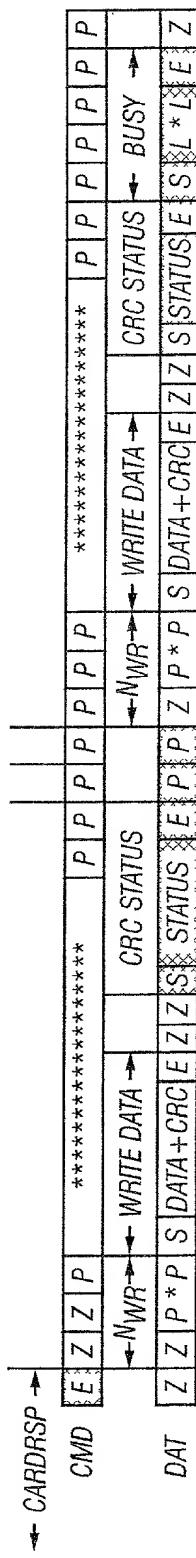


FIG. 32

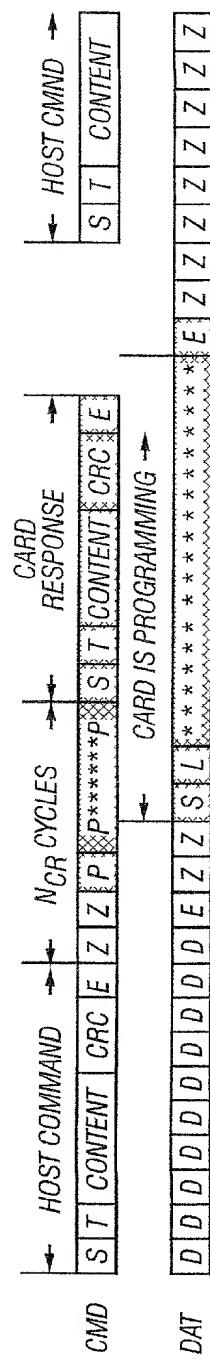
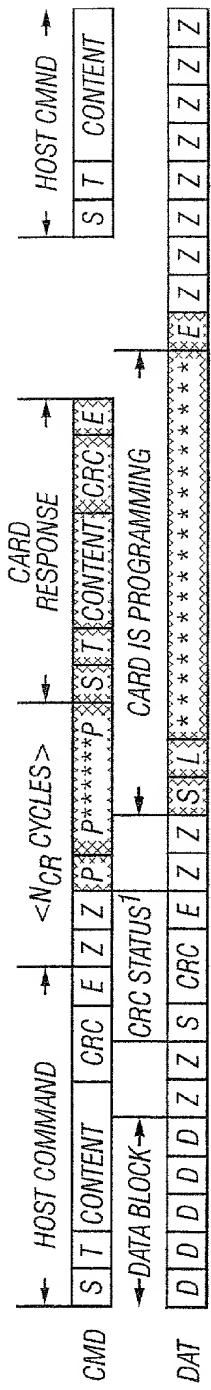
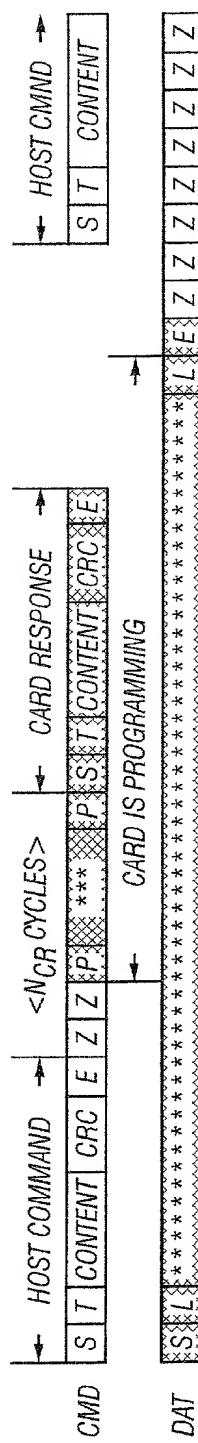


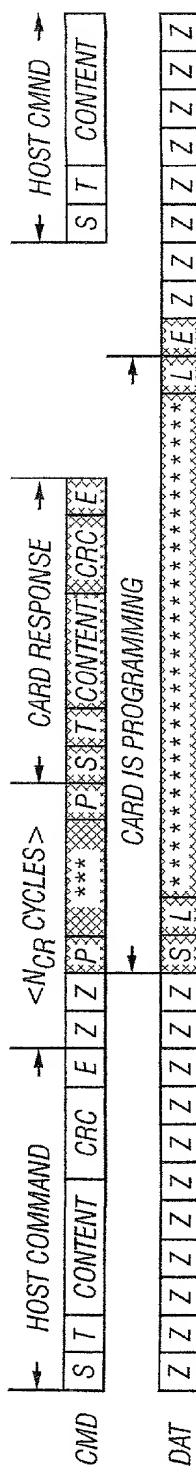
FIG. 33



1) THE CARD CRC STATUS RESPONSE WAS INTERRUPTED BY THE HOST.



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COMMAND CLASS (CCC)	CLASS DESCRIPTION	0	1	2	3	4	7	9	10	11	12	13	15	16	17	18	20
CLASS 0	BASIC	+	+	+	+	+	+	+	+	+	+	+					
CLASS 1	STREAM READ									+							
CLASS 2	BLOCK READ												+	+	+		
CLASS 3	STREAM WRITE																+
CLASS 4	BLOCK WRITE													+			
CLASS 5	ERASE																
CLASS 6	WRITE WRITE-PROTECTION																
CLASS 7	READ WRITE-PROTECTION																
CLASS 8	ERASE WRITE-PROTECTION																
CLASS 9	I/O MODE																
CLASS 10-11	RESERVED																

CARD COMMAND CLASS (CCC)	CLASS DESCRIPTION	SUPPORTED COMMANDS															
		24	25	26	27	28	29	30	32	33	34	35	36	37	38	39	40
CLASS 0	BASIC																
CLASS 1	STREAM READ																
CLASS 2	BLOCK READ																
CLASS 3	STREAM WRITE																
CLASS 4	BLOCK WRITE	+	+	+	+												
CLASS 5	ERASE										+	+	+	+	+	+	+
CLASS 6	WRITE WRITE-PROTECTION								+	+							
CLASS 7	READ WRITE-PROTECTION										+						
CLASS 8	ERASE WRITE-PROTECTION									+	+	+					
CLASS 9	I/O MODE															+	+
CLASS 10-11	RESERVED																

FIG. 37

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD0	BC	[31:0] STUFF BITS	-	GO_IDLE_STATE	RESETS ALL CARDS TO IDLE STATE
CMD1	BCR	[31:0] OCR WITHOUT BUSY	R3	SEND_OP_COND	ASKS ALL CARDS IN IDLE STATE TO SEND THEIR OPERATION CONDITIONS REGISTER CONTENTS IN THE RESPONSE ON THE CMD LINE
CMD2	BCR	[31:0] STUFF BITS	R2	ALL_SEND_CID	ASKS ALL CARDS TO SEND THEIR CID NUMBERS ON THE CMD LINE
CMD3	AC	[31:16] RCA	R1	SET_RELATIVE_ADDR	ASSIGNS RELATIVE ADDRESS TO THE CARD
CMD4	BC	[15:0] STUFF BITS	-	SET_DSR	PROGRAMS THE DSR OF ALL CARDS
CMD5	RESERVED				
CMD6	RESERVED				
CMD7	AC	[31:16] RCA [15:0] STUFF BITS	R1 (ONLY FROM THE SELECTED CARD)	SELECT_CARD DESELECT_CARD	COMMAND TOUGLES A CARD BETWEEN THE STAND-BY AND TRANSFER STATES OR BETWEEN THE PROGRAMMING AND DISCONNECT STATES. IN BOTH CASES THE CARD IS SELECTED BY ITS OWN RELATIVE ADDRESS AND GETS DESELECTED BY ANY OTHER ADDRESS; ADDRESS 0 DESELECTS ALL.
CMD8	RESERVED				
CMD9	AC	[31:16] RCA [15:0] STUFF BITS	R2	SEND_CSD	ADDRESSED CARD SENDS ITS CARD-SPECIFIC DATA (CSD) ON THE CMD LINE
CMD10	AC	[31:16] RCA [15:0] STUFF BITS	R2	SEND_CID	ADDRESSED CARD SENDS ITS CARD IDENTIFICATION (CID) ON THE CMD LINE
CMD11	ADTC	[31:0] DATA ADDRESS1	R1	READ_DAT_UNTIL_STOP	READS DATA STREAM FROM THE CARD, STARTING AT THE GIVEN ADDRESS, UNTIL A STOP TRANSMISSION FOLLOWS
CMD12	AC	[31:0] STUFF BITS	R1	STOP_TRANSMISSION	FORCES THE CARD TO STOP TRANSMISSION

FIG. 38A

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD13	AC	[31:16] RCA [15:0] STUFF BITS	R1	SEND_STATUS	ADDRESSED CARD SENDS ITS STATUS REGISTER.
CMD14	RESERVED				
CMD15	AC	[31:16] RCA [15:0] STUFF BITS	-	GO_INACTIVE_STATE	SETS THE CARD TO INACTIVE STATE IN ORDER TO PROTECT THE CARD STACK AGAINST COMMUNICATION BREAKDOWNS.

FIG. 38B

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD16	AC	[31:0] BLOCK LENGTH	R1	SET_BLOCKLEN	SETS THE BLOCK LENGTH (IN BYTES) FOR ALL FOLLOWING BLOCK COMMANDS (READ AND WRITE). DEFAULT BLOCK LENGTH IS SPECIFIED IN THE CSD.
CMD17	ADTC	[31:0] DATA ADDRESS	R1	READ_SINGLE_BLOCK	READS A BLOCK OF THE SIZE SELECTED BY THE SET_BLOCKLEN COMMAND. ¹
CMD18	ADTC	[31:0] DATA ADDRESS	R1	READ_MULTIPLE_BLOCK	CONTINUOUSLY TRANSFERS DATA BLOCKS FROM CARD TO HOST UNTIL INTERRUPTED BY A STOP COMMAND.
CMD19	RESERVED				

FIG. 39

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD20	ADTC	[31:0] DATA ADDRESS	R1B	WRITE_DAT_STOP	WRITES DATA STREAM FROM THE HOST, STARTING AT THE GIVEN ADDRESS, UNTIL A STOP_TRANSMISSION FOLLOWS.
CMD21	RESERVED				
CMD23	RESERVED				

FIG. 40

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD24	ADTC	[31:0] DATA ADDRESS	R1B	WRITE_BLOCK	WRITES A BLOCK OF THE SIZE SELECTED BY THE SET_BLOCKEN COMMAND.
CMD25	ADTC	[31:0] DATA ADDRESS	R1B	WRITE_MULTIPLE_BLOCK	CONTINUOUSLY WRITES BLOCKS OF DATA UNTIL A STOP_TRANSMISSION FOLLOWS.
CMD26	ADTC	[31:0] STUFF BITS	R1B	PROGRAM_CD	PROGRAMMING OF THE CARD IDENTIFICATION REGISTER. THIS COMMAND SHALL BE ISSUED ONLY ONCE PER MMC CARD. THE CARD CONTAINS HARDWARE TO PREVENT THIS OPERATION AFTER THE FIRST PROGRAMMING. NORMALLY THIS COMMAND IS RESERVED FOR THE MANUFACTURER
CMD27	ADTC	[31:0] STUFF BITS	R1B	PROGRAM_CSD	PROGRAMMING OF THE PROGRAMMABLE BITS OF THE CSD.

FIG. 41

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD28	AC	[31:0] DATA ADDRESS	R1B	SET_WRITE_PROT	<i>IF THE CARD HAS WRITE PROTECTION FEATURES, THIS COMMAND SETS THE WRITE PROTECTION BIT OF THE ADDRESSED GROUP. THE PROPERTIES OF WRITE PROTECTION ARE CODED IN THE CARD SPECIFIC DATA (WP_GRP_SIZE).</i>
CMD29	AC	[31:0] DATA ADDRESS	R1B	CLR_WRITE_PROT	<i>IF THE CARD PROVIDES WRITE PROTECTION FEATURES, THIS COMMAND CLEARS THE WRITE PROTECTION BIT OF THE ADDRESSED GROUP.</i>
CMD30	ADTC	[31:0] WRITE PROTECT DATA ADDRESS	R1	SEND_WRITE_PROT	<i>IF THE CARD PROVIDES WRITE PROTECTION FEATURES, THIS COMMAND ASKS THE CARD TO SEND THE STATUS OF THE WRITE PROTECTION BITS.</i>
CMD31	RESERVED				

FIG. 42

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD32	AC	[31:0] DATA ADDRESS	R1	TAG_SECTOR_START	SETS THE ADDRESS OF THE FIRST SECTOR OF THE ERASE GROUP.
CMD33	AC	[31:0] DATA ADDRESS	R1	TAG_SECTOR_END	SETS THE ADDRESS OF THE LAST SECTOR IN A CONTINUOUS RANGE WITHIN THE SELECTED ERASE GROUP OR THE ADDRESS OF A SINGLE SECTOR TO BE SELECTED FOR ERASE.
CMD34	AC	[31:0] DATA ADDRESS	R1	UNTAG_SECTOR	REMOVES ONE PREVIOUSLY SELECTED SECTOR FROM THE ERASE SELECTION.
CMD35	AC	[31:0] DATA ADDRESS	R1	TAG_ERASE_GROUP_START	SETS THE ADDRESS OF THE FIRST ERASE GROUP WITHIN A RANGE TO BE SELECTED FOR ERASE.
CMD36	AC	[31:0] DATA ADDRESS	R1	TAG_ERASE_GROUP_END	SETS THE ADDRESS OF THE LAST ERASE GROUP WITHIN A CONTINUOUS RANGE TO BE SELECTED FOR ERASE.
CMD37	AC	[31:0] DATA ADDRESS	R1	UNTAG_ERASE_GROUP	REMOVES ONE PREVIOUSLY SELECTED ERASE GROUP FROM THE ERASE SELECTION.
CMD38	AC	[31:0] STUFF BITS	R1B	ERASE	ERASES ALL PREVIOUSLY SELECTED SECTORS

FIG. 43

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD39	AC	[31:16] RCA [15:8] REGISTER ADDRESS [7:0] REGISTER DATA	R4	FAST_J0	USED TO WRITE AND READ 8 BIT (REGISTER) DATA FIELDS. THE COMMAND ADDRESSES A CARD AND A REGISTER AND PROVIDES THE DATA. THE R4 RESPONSE CONTAINS DATA READ FROM THE ADDRESSED REGISTER. THIS COMMAND ACCESSES APPLICATION DEPENDENT REGISTERS WHICH ARE NOT DEFINED IN THE MMC STANDARD.
CMD40	BCR	[31:0] STUFF BITS	R5	GO IRQ STATE	SETS THE SYSTEM INTO INTERRUPT MODE
CMD41- CMD59	RESERVED				
CMD60- 63	RESERVED FOR MANUFACTURER				

FIG. 44

BIT POSITION	47	46	[45:40]	[39:8]	[7:1]	0
WIDTH (BITS)	1	1	6	32	7	1
VALUE	'0'	'0'	X	X	X	'1'
DESCRIPTION	START BIT	TRANSMISSION BIT	COMMAND INDEX	CARD STATUS	CRC7	END BIT

FIG. 45

BIT POSITION	135	134	[133:128]	[127:1]	0
WIDTH (BITS)	1	1	6	127	1
VALUE	'0'	'0'	'111111'	X	'1'
DESCRIPTION	START BIT	TRANSMISSION BIT	RESERVED	CID OR CSD REGISTER INCL INTERNAL CRC7	END BIT

FIG. 46

BIT POSITION	47	46	[45:40]	[39:8]	[7:1]	0
WIDTH (BITS)	1	1	6	32	7	1
VALUE	'0'	'0'	'111111'	X	'1111111'	'1'
DESCRIPTION	START BIT	TRANSMISSION BIT	RESERVED	OCR REGISTER	RESERVED	END BIT

FIG. 47

BIT POSITION	47	46	[45:40]	[39:8]	ARGUMENT FIELD	[7:1]	0
WIDTH (BITS)	1	1	6	16	8	8	7
VALUE	'0'	'000111'	X	X	X	X	'1'
DESCRIPTION	START BIT	TRANSMISSION BIT	CMD39 [31:16]	RCA REGISTER ADDR. [15:8]	READ REGISTER CONTENTS [7:0]	CRC7	END BIT

FIG. 48

BIT POSITION	47	46	[45:40]	[39:8] ARGUMENT FIELD		[7:1]	0
WIDTH (BITS)	1	1	6	16		7	1
VALUE	'0'	'0'	'101000'	X	X	X	'1'
DESCRIPTION	START BIT	TRANSMISSION BIT	CMD40	RCA [31:16] OF WINNING CARD OR OF THE HOST	[15:0] NOT DEFINED. MAY BE USED FOR IRQ DATA	CRC7	END BIT

FIG. 49

BITS	IDENTIFIER	TYPE	VALUE	DESCRIPTION	CLEAR CONDITION
31	OUT_OF_RANGE	ER	'0'=NO ERROR '1'=ERROR	THE COMMAND'S ARGUMENT WAS OUT OF THE ALLOWED RANGE FOR THIS CARD.	C
30	ADDRESS_ERROR	ERX	'0'=NO ERROR '1'=ERROR	A MISALIGNED ADDRESS WHICH DID NOT MATCH THE BLOCK LENGTH WAS USED IN THE COMMAND.	C
29	BLOCK_LEN_ERROR	ER	'0'=NO ERROR '1'=ERROR	THE TRANSFERRED BLOCK LENGTH IS NOT ALLOWED FOR THIS CARD, OR THE NUMBER OF TRANSFERRED BYTES DOES NOT MATCH THE BLOCK LENGTH.	C
28	ERASE_SEQ_ERROR	ER	'0'=NO ERROR '1'=ERROR	AN ERROR IN THE SEQUENCE OF ERASE COMMANDS OCCURRED.	C
27	ERASE_PARAM	EX	'0'=NO ERROR '1'=ERROR	AN INVALID SELECTION OF SECTORS OR GROUPS FOR ERASE OCCURRED.	C
26	WP_VIOLATION	ERX	'0'=NOT PROTECTED '1'=PROTECTED	ATTEMPT TO PROGRAM A WRITE PROTECTED BLOCK.	C
25 24	RESERVED				
23	COM_CRC_ERROR	ER	'0'=NO ERROR '1'=ERROR	THE CRC CHECK OF THE PREVIOUS COMMAND FAILED.	B
22	ILLEGAL_COMMAND	ER	'0'=NO ERROR '1'=ERROR	COMMAND NOT LEGAL FOR THE CARD STATE	B
21	CARD_ECC_FAILED	EX	'0'=SUCCESS '1'=FAILURE	CARD INTERNAL ECC WAS APPLIED BUT FAILED TO CORRECT THE DATA.	C
20	CC_ERROR	ERX	'0'=NO ERROR '1'=ERROR	INTERNAL CARD CONTROLLER ERROR	C
19	ERROR	ERX	'0'=NO ERROR '1'=ERROR	A GENERAL OR AN UNKNOWN ERROR OCCURRED DURING THE OPERATION.	C
18	UNDERRUN	EX	'0'=NO ERROR '1'=ERROR	THE CARD COULD NOT SUSTAIN DATA PROGRAMMING IN STREAM READ MODE	C
17	OVERRUN	EX	'0'=NO ERROR '1'=ERROR	THE CARD COULD NOT SUSTAIN DATA PROGRAMMING IN STREAM WRITE MODE	C
16	CID/ CSD_OVERWRITE	ER	'0'=NO ERROR '1'=ERROR	CAN BE EITHER ONE OF THE FOLLOWING ERRORS: -THE CID REGISTER HAS BEEN ALREADY WRITTEN AND CAN NOT BE OVERWRITTEN -THE READ ONLY SECTION OF THE CSD DOES NOT MATCH THE CARD CONTENT. -AN ATTEMPT TO REVERSE THE COPY (SET AS ORIGINAL) OR PERMANENT WP (UNPROTECTED)BITS WAS MADE.	C

FIG. 50A

BITS	IDENTIFIER	TYPE	VALUE	DESCRIPTION	CLEAR CONDITION
15	WP_ERASE_SKIP	SX	'0'=NOT PROTECTED '1'=PROTECTED	ONLY PARTIAL ADDRESS SPACE WAS ERASED DUE TO EXISTING WRITE PROTECTED BLOCKS.	C
14	CARD_ECC_DISABLED	SX	'0'=ENABLED '1'=DISABLED	THE COMMAND HAS BEEN EXECUTED WITHOUT USING THE INTERNAL ECC.	A
13	ERASE_RESET	SR	'0'=Cleared '1'=SET	AN ERASE SEQUENCE WAS CLEARED BEFORE EXECUTING BECAUSE AN OUT OF ERASE SEQUENCE COMMAND WAS RECEIVED	C
12:9	CURRENT_STATE	SX	0=IDLE 1=READY 2=IDENT 3=STBY 4=TRAN 5=DATA 6=RCV 7=PRG 8=DIS 9-15=RESERVED	STATE OF THE CARD. THE FOUR BITS ARE INTERPRETED AS A BINARY CODED NUMBER BETWEEN 0 AND 15.	B
8	READY_FOR_DATA	SX	'0'=NOT READY '1'=READY	CORRESPONDS TO BUFFER EMPTY SIGNALING ON THE BUS	A
70	RESERVED				

FIG. 50B

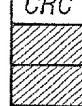
S	START BIT (=0')
T	TRANSMITTER BIT (HOST='1', CARD='0')
P	ONE-CYCLE PULL-UP (=1')
E	END BIT (=1)
Z	HIGH IMPEDANCE STATE (->='1')
D	DATA BITS
*	REPETITION
CRC	CYCLIC REDUNDANCY CHECK BITS (7 BITS)
	CARD ACTIVE
	HOST ACTIVE

FIG. 51

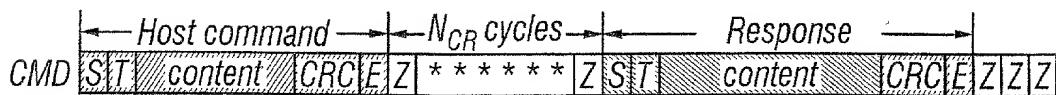


FIG. 52

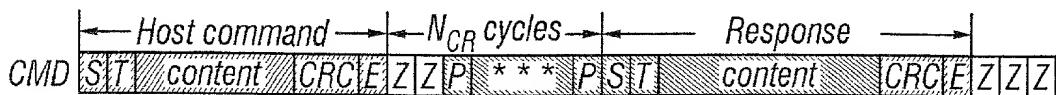


FIG. 53

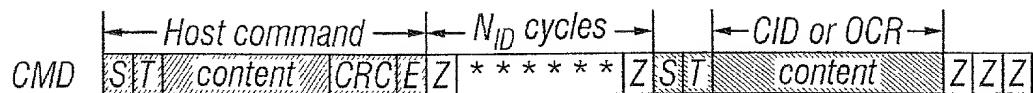


FIG. 54

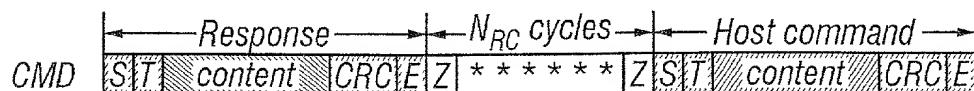


FIG. 55

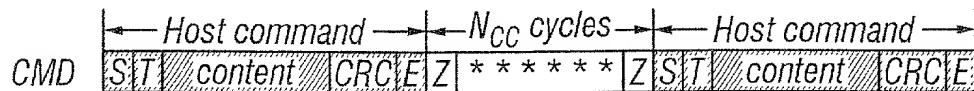


FIG. 56

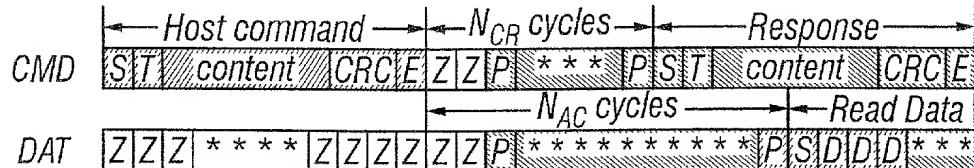


FIG. 57

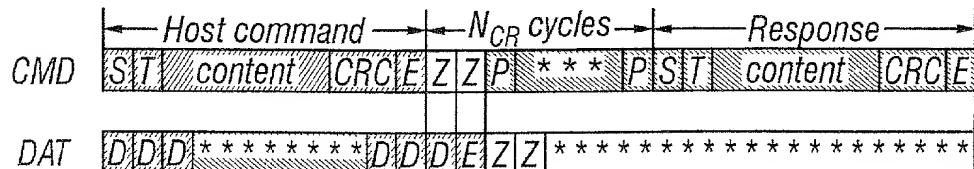


FIG. 58

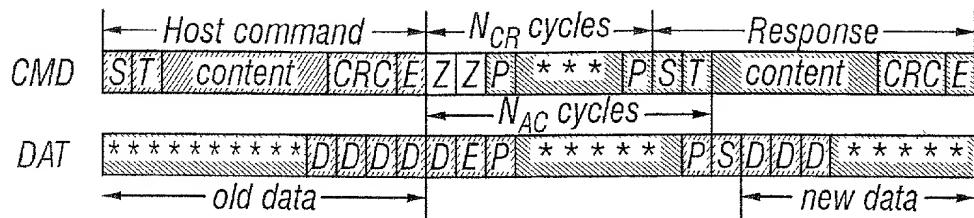


FIG. 59

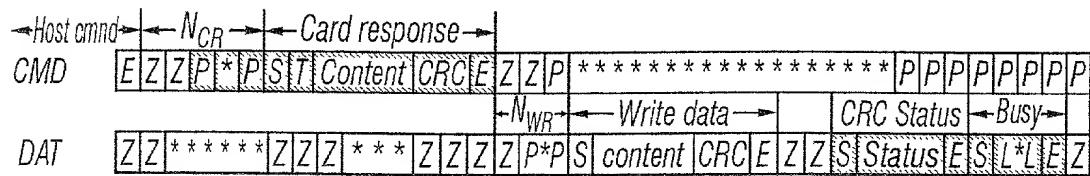


FIG. 60

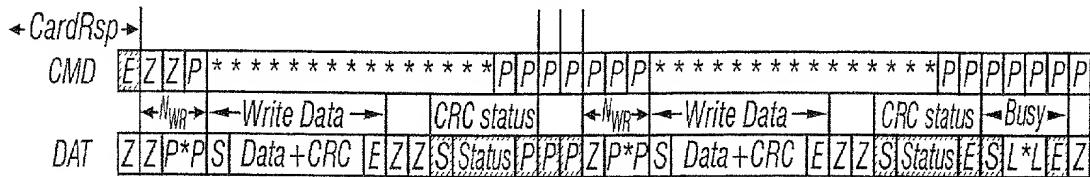


FIG. 61

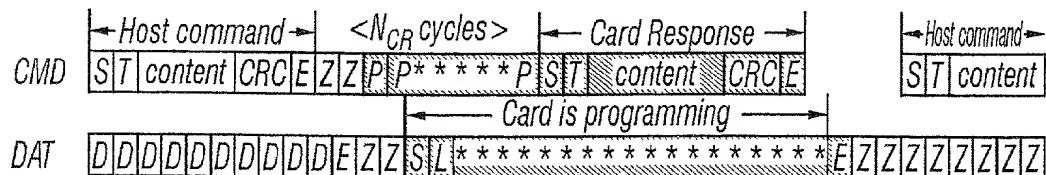


FIG. 62

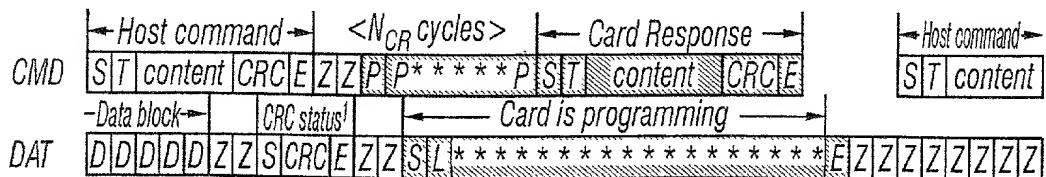


FIG. 63

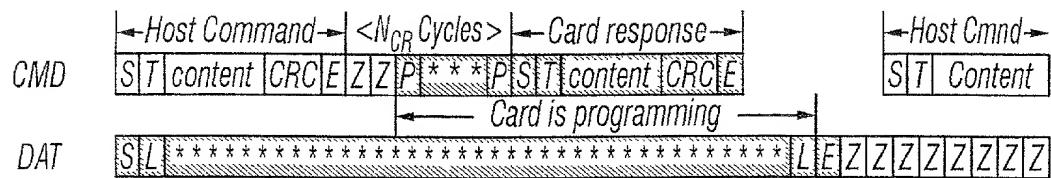


FIG. 64

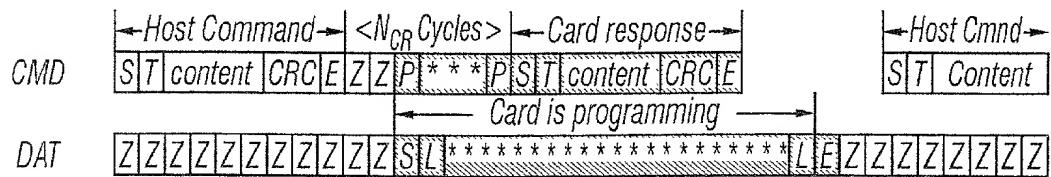


FIG. 65

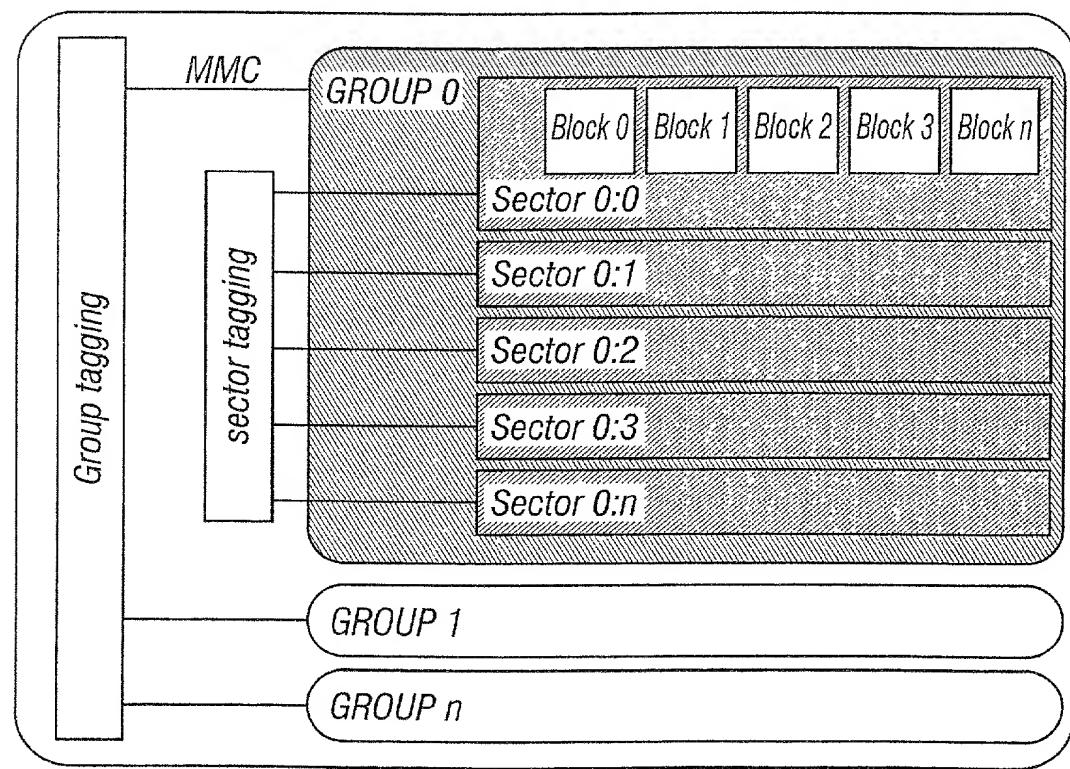


FIG. 66

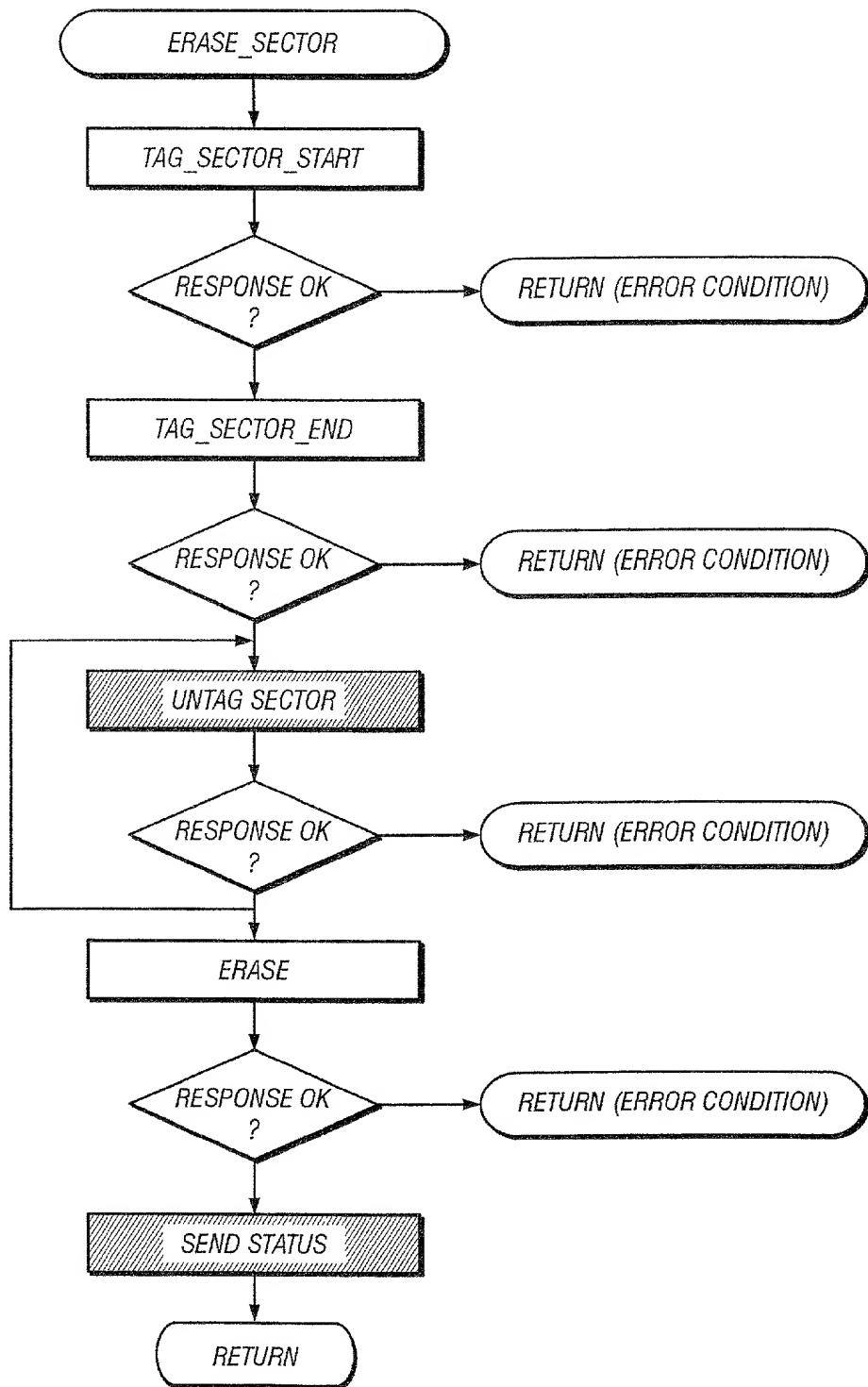


FIG. 67

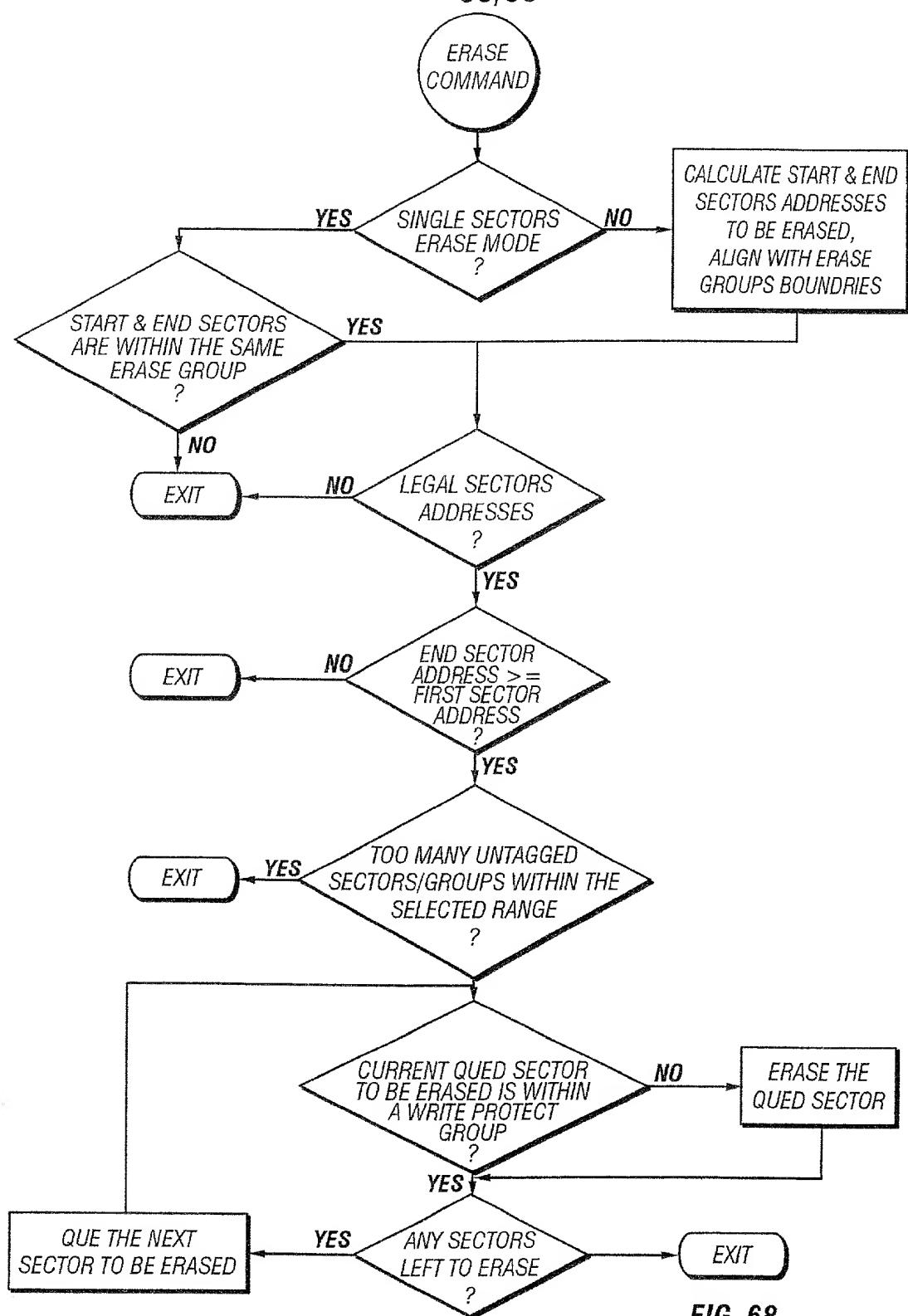


FIG. 68

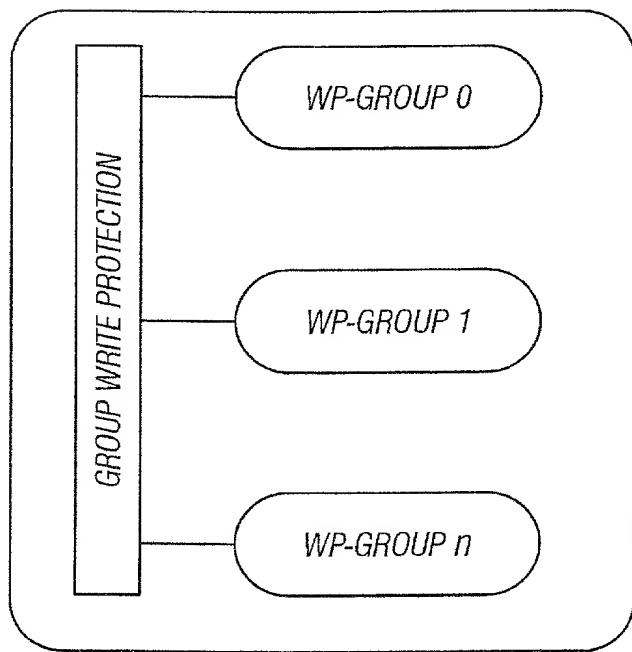


FIG. 69

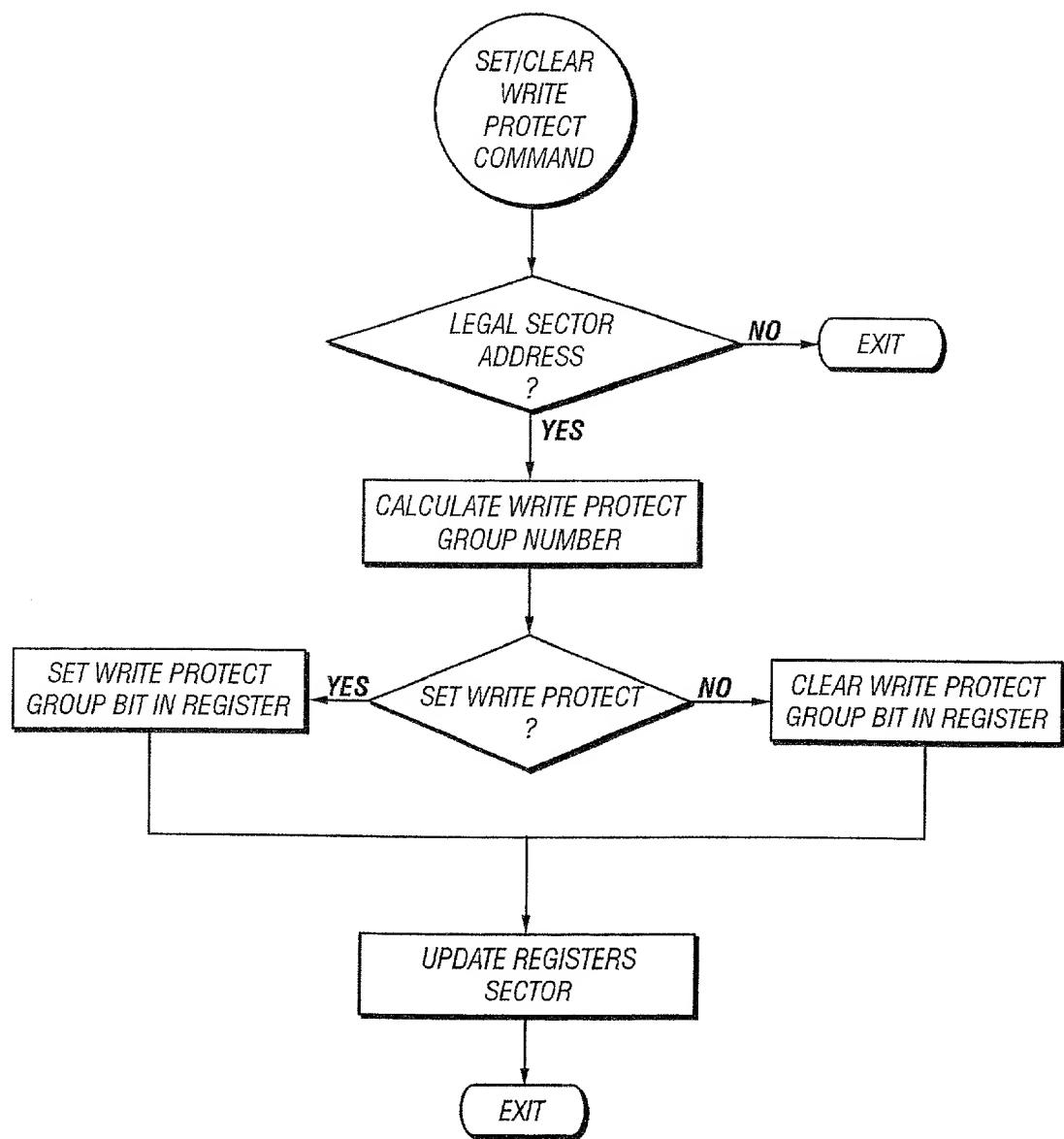


FIG. 70

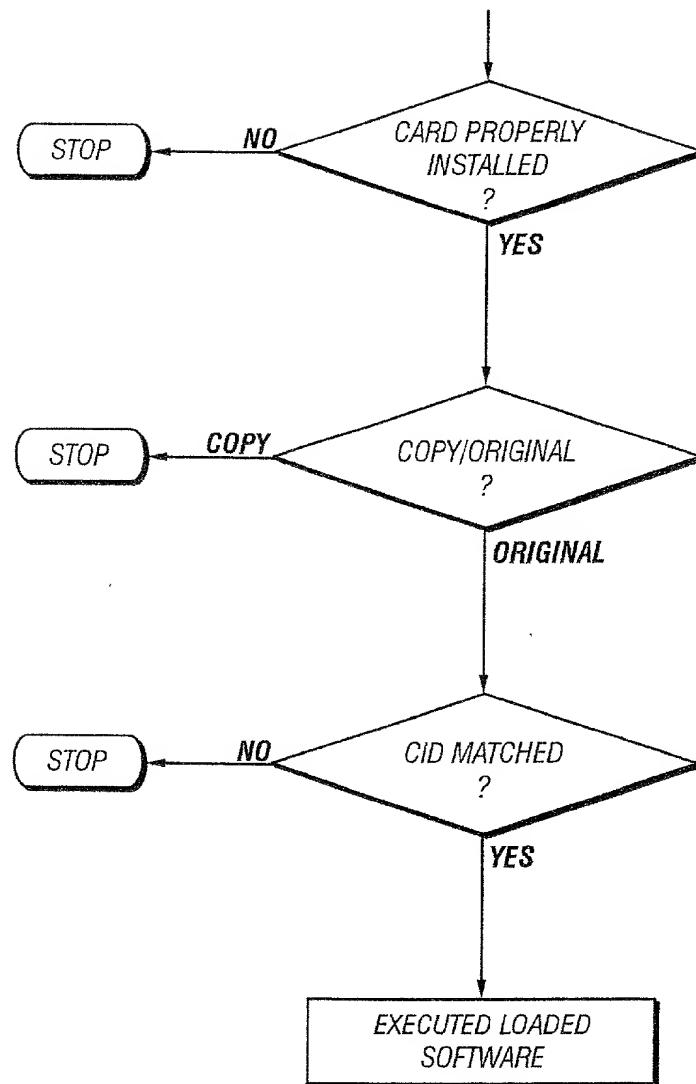


FIG. 71